METHOD FOR AMPLITUDE INSENSITIVE PACKET DETECTION

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The invention relates generally to the field of wireless communications and more particularly to a method of and device for detecting the presence of a received data packet in a digital receiver.

Description of the Related Prior Art

[0002] Rapid growth in the portable communications market has pushed designers to seek low-cost, low-power, highly integrated solutions for the radio frequency (RF) transceiver in accordance with the IEEE 802.11a-1999 Part 11: "Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications – High Speed Physical Layer in the 5GHz Band which is incorporated herein by reference. As those skilled in the art will appreciate, an important aspect of any wireless receiver is the ability to detect the presence of data packets where the received signal may be degraded as a result of multi-path fading and/or the presence of noise.

[0003] A wireless radio receiver employing digital demodulation methods typically detects the presence of energy in order to start a timing machine to control the proper acquisition of the radio signal. This acquisition typically involves determining a radio frequency preamble or known 'signature' signal.

[0004] Acquisition involves applying the input signal to a filter "matched" to the

original RF signature and examining the matched filter output for a "peak" to signify that a signal with a valid signature was detected. As will be appreciated by those in the art, certain radio frequency applications perform signal processing operations by separating radio frequency signals into signal components representing in-phase (I) and quadrature (Q) channels (I/Q channels). If the RF signal is demodulated to complex I/Q baseband then the matched filter must also be complex I/Q at baseband. This process is defined as "complex matched filter correlation" or "correlation" for short.

[0005] If the radio signal undergoes rapid automatic gain control (AGC) fluctuation during the acquisition process, then the quality of the correlation peak will deteriorate and the determination of a valid signature may be compromised. As those in the art will appreciate, an AGC circuit is a circuit by which gain is automatically adjusted in a specific manner as a function of a specified parameter, such as received signal strength (RSSI).

[0006] Past solutions normalize the baseband I or Q signals by dividing by an estimate of the AGC gain in a receiver line-up. The problem with this approach is that it requires an estimate of the gain value. This gain estimate takes time, and is usually noisy if limited time is available, so in applications where limited time is available (as in IEEE 802.11a) a poor estimate must be used, resulting in a noisy correlator output and an increased probability of false detection.

[0007] The poor gain estimate means that a conventional normalization will create a correlator output that is either too large or too small depending on the difference between the magnitude of the input signal and the value of the gain estimate.

SUMMARY OF THE INVENTION

[0008] In order to overcome the deficiencies of the prior art there is provided a simplified method of correlation which eliminates dependency on input signal amplitude fluctuations while at the same time maintaining phase relevancy, which is important for

the correlation process. The present invention removes the requirement for full normalization, which is usually done by a complex multiplier circuit and replaces it with a simple look-up table (LUT) with M discrete complex I/Q phase outputs.

[0009] In accordance with one aspect of the invention there is provided in a digital wireless receiver, a method of detecting the presence of a data packet in a received radio frequency (RF) signal comprising the steps of: separating the RF signal into in-phase (I) and quadrature (Q) signals; removing direct current (DC) offsets from the I and Q signals; modulating the I and Q signals; performing amplitude normalization on said modulated I and Q signals; comparing said amplitude normalized I and Q signals to a reference signal via a complex correlator; detecting a peak of said complex correlator output; and if said peak is above a predefined threshold, indicating that a data packet has been received, else performing steps (a) to (g) on a subsequently received RF signal.

[00010] Preferably, the step of performing amplitude normalization comprises mapping said modulated I and Q signals to a quantized phase shift keying (PSK) signal constellation.

[00011] In accordance with a second aspect of the invention, there is provided in a wireless digital receiver, a circuit for detecting the presence of a data packet in a received radio frequency (RF) signal comprising: a direct current (DC) offset module to correct for local oscillator (LO) leakage in in-phase (I) and quadrature (Q) signals derived from the received RF signal; an acquisition module communicating with the DC offset module comprising: a M-ary phase shift keying (PSK) mapper for mapping the I and Q signals to a quantized PSK signal constellation; a complex correlator receiving input from the M-ary PSK mapper for comparing the mapped I and Q signals to a reference; and a detector receiving input from the complex correlator for determining the presence of a correct signature.

[00012] Preferably, the detector further comprises: a complex to polar (C2P)

stream converter for converting the output of the complex correlator into an amplitude and phase value; a magnitude calculation module for determining a signal size of the converted output; and a peak detection module communicating with the magnitude calculation module for determining the presence of information bits.

The advantages of the invention are now readily apparent. This simplified normalization scheme makes the algorithm robust against amplitude variations in the input signal, while still allowing for good correlation output. In applications where interference is superimposed on the I/Q input signals, the invention improves the detection capability over AGC normalization methods.

BRIEF DESCRIPTION OF THE DRAWINGS

[00013] A better understanding of the invention will be obtained by considering the detailed description below, with reference to the following drawings in which:

Figure 1 is a block diagram of a digital receiver;

Figure 2 is a block diagram of digital demodulator contained in the digital receiver of Figure 1;

Figure 3 is a block diagram of the digital demodulator front-end contained in the digital demodulator of Figure 2;

Figure 4 is a block diagram of the packet detection system of the present invention contained in the digital demodulator front-end of Figure 3;

Figure 5 is a block diagram of the acquisition block of the packet detection system of Figure 4;

Figure 6 is an I/Q signal constellation; and

Figure 7 is a block diagram of the detector contained in the acquisition block of Figure 5.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[00014] Referring to Figure 1, there is depicted a digital receiver 10 in which the present invention is housed. The preferred digital receiver 10 may be, for example, the ICE5350 Digital Receiver offered by IceFyre Semiconductor Inc. which performs all the physical layer functions detailed in the IEEE 802.11a standard, but the invention is not meant to be limited to this receiver. The digital receiver 10 is located between the RF Receiver Front End 12 and the Physical Medium Access Control (PHY/MAC) 14. The RF Receiver Front End 12 connects to antennae A and B. As shown in the drawing, the two main blocks within the digital receiver 10 are the digital demodulator 16 and the baseband decoder 18. The digital demodulator 16 recovers the baseband signal by removing carrier offsets, timing offsets, compensating for the channel impairments and demapping the digitally modulated signal. This block is located between the analog-to-digital interface (not shown) and the baseband interface (not shown). The baseband decoder 18 de-interleaves the baseband signal, provides error correction through the soft-decision Viterbi algorithm and unscrambles the corrected bit stream to be passed through the PHY/MAC 14. This block is located between the baseband interface (not shown) and the PHY/MAC interface (not shown).

[00015] Figure 2 depicts the digital demodulator 16 of Figure 1. As shown in the diagram, the analog to digital interface is located at block ADCs/ DACs 20. The baseband interface can also be seen in the figure at the soft decision demapper 22. It can also be seen in the figure that the digital demodulator 16 is distinctly divided into two parts by the Fast Fourier Transform (FFT) circuit 24. To the left is the digital demodulator front-end (DFE) 26, while to the right is the digital demodulator back-end (DBE) 28. The invention of the present invention is provided in the digital demodulator front-end 26.

[00016] Figure 3 provides a more detailed overview of the digital demodulator

front-end 26. As depicted in the Figure, there are four main processing paths in the front-end (shown in circled numbers 1 to 4):

1) Signal detection path, the purpose of which is to determine when a burst is present and select the best antenna for use;
2) SHORT symbol correlation path, the purpose of which is to determine burst timing and make a course frequency estimate and pass the estimate to the analog block local oscillator;
3) LONG symbol correlation path, the purpose of which is to make a fine frequency estimate and initialize the digital local oscillator; and
4) Data detection path, the purpose of which is to down-sample the orthogonal frequency division multiplexed (OFDM) symbols, correct the center frequency, and remove the Guard Interval (GI).

The present invention pertains to the data detection path.

[00017] Figure 4 is a block diagram of the packet detection system of the present invention. As indicated above, the present invention proposes a simplified method of correlation by removing dependency on the input RF signal amplitude fluctuations while at the same time maintaining phase relevancy. The key advancement involves mapping the complex quadrature amplitude modulation (QAM) preamble to a quantized phase shift keying (PSK) constellation before application to a matched complex correlator. This process essentially "amplitude normalizes" the input signal without the use or complexity associated with a divider. As will be discussed in greater detail in relation to Figure 5, the output from the PSK mapper may take any one of M phases on the unit circle, but only has a unity magnitude.

[00018] More specifically, as shown in Figure 4, the system comprises I and Q direct current (DC) offset modules 30, 32 and acquisition block 34. Each of the I and Q signals must have DC offsets removed to some degree since DC offsets may skew the performance of the acquisition block. As those skilled in the art will appreciate, DC offsets arise from local oscillator (LO) leakage or feedthrough. The leakage signal is mixed with the LO signal thereby producing a DC component. If directly amplified, the

offset voltage can saturate the circuit, prohibiting the amplification of the desired signal. Therefore some means of offset cancellation is required. DC estimation modules 36, 38 estimate the required offset which is applied to the incoming I and Q signals. As those in the art will understand, one method of offset cancellation involves exploiting the idle time intervals in digital wireless standards to carry out offset cancellations.

[00019] The acquisition module is depicted in Figure 5 and consists of a M-ary Phase Shift Keying (PSK) phase mapper 40, a complex correlator 42 and a detector 44. In digital RF systems, the carrier is modulated by a digital baseband signal. One such modulation technique known in the art is phase shift keying in which the phase of a carrier is discretely varied in relation either to a reference phase or the phase of the immediately preceding signal element, in accordance with the data being transmitted. The simplest method, binary PSK (BPSK) uses only two signal phases: 0 and 180 degrees. It is sometimes advantageous to employ multilevel digital signals (as opposed to binary signals) to modulate the carrier. This form of signaling is called M–ary signaling, where M is a parameter representing the number of phases chosen. M-ary PSK used in the present invention is a multilevel modulation technique in which multiple phase angles are modulated (e.g. 0, +45, -45, +90, -90, +135, -135, 180).

[00020] As indicated in the background section, after demodulation, the received signal is down-converted to an in-phase (I) and a quadrature (Q) baseband component, representing the amplitude of cosine and sine components respectively. It is very helpful to view these signals on a so-called "constellation" diagram, also known as a polar plot or Argand diagram - a 2-dimensional representation with in-phase (I) on the X axis and quadrature (Q) on the Y axis. At any instant, the signal's two values can be represented by a point on this X/Y plot. In the case of the present invention, M-ary PSK phase mapper 42 maps a particular I/Q constellation point to a defined output I/Q lying on the unit circle as shown in Figure 6. As seen in figure 6, several mappings which serve to quantize the phase angle and limit the amplitude to "1" are depicted. The process essentially "amplitude normalizes" the input signal without the requirement for additional components. Better performance can be obtained by increasing the number of phases M in the M-ary PSK mapper 42.

[00021] Following the M-ary PSK mapper 42 is a complex correlator 44 which compares the output of the M-ary PSK mapper 42 to a stored replica of a correct (i.e. noiseless) reference signal. The detector 46, more fully depicted in Figure 7 is used to convert the output of the complex correlator 44 to a magnitude and detect a peak. If the peak is above a predefined threshold, then packet detection is declared. Detector 46 comprises a complex to polar (C2P) converter 48, which converts each value received from complex correlator 44 into an amplitude and phase value. The magnitude output of C2P 48 is fed to an optional magnitude calculation module 50 which calculates a signal power according to the formula (mag)^2. Calculation of the squared magnitude is not absolutely necessary, for example, the magnitude could be used in some applications. The output of module 50 is then fed to peak detection module 52 which determines whether or not the correlator peak magnitude exceeds some minimum predfeined threshold. If this minimum threshold is exceeded, then it indicates that the correct "signature" was received and that information bits are present. Fast peak detection techniques are available such as peak signal envelope detection and these are known to those in the art and meant to be included within the scope of the invention.

[00022] As will be understood by those skilled in the art, the present invention relates to integrated circuits in which a packet detection circuit is used in combination with other components to perform a useful function within an integrated circuit. The individual electronic and processing functions utilized in the foregoing described embodiment are, individually, well understood by those skilled in the art. It is to be understood by the reader that a variety of other implementations may be devised by skilled persons for substitution and the claimed invention herein is intended to encompass all such alternative implementations, substitutions and equivalents. Persons skilled in the field of radio frequency and integrated circuit design will be readily able to apply the present invention to an appropriate implementation for a given application.

[00023] Consequently, it is to be understood that the particular embodiments

shown and described herein by way of illustration are not intended to limit the scope of the invention claimed by the inventors/assignee, which is defined by the appended claims.